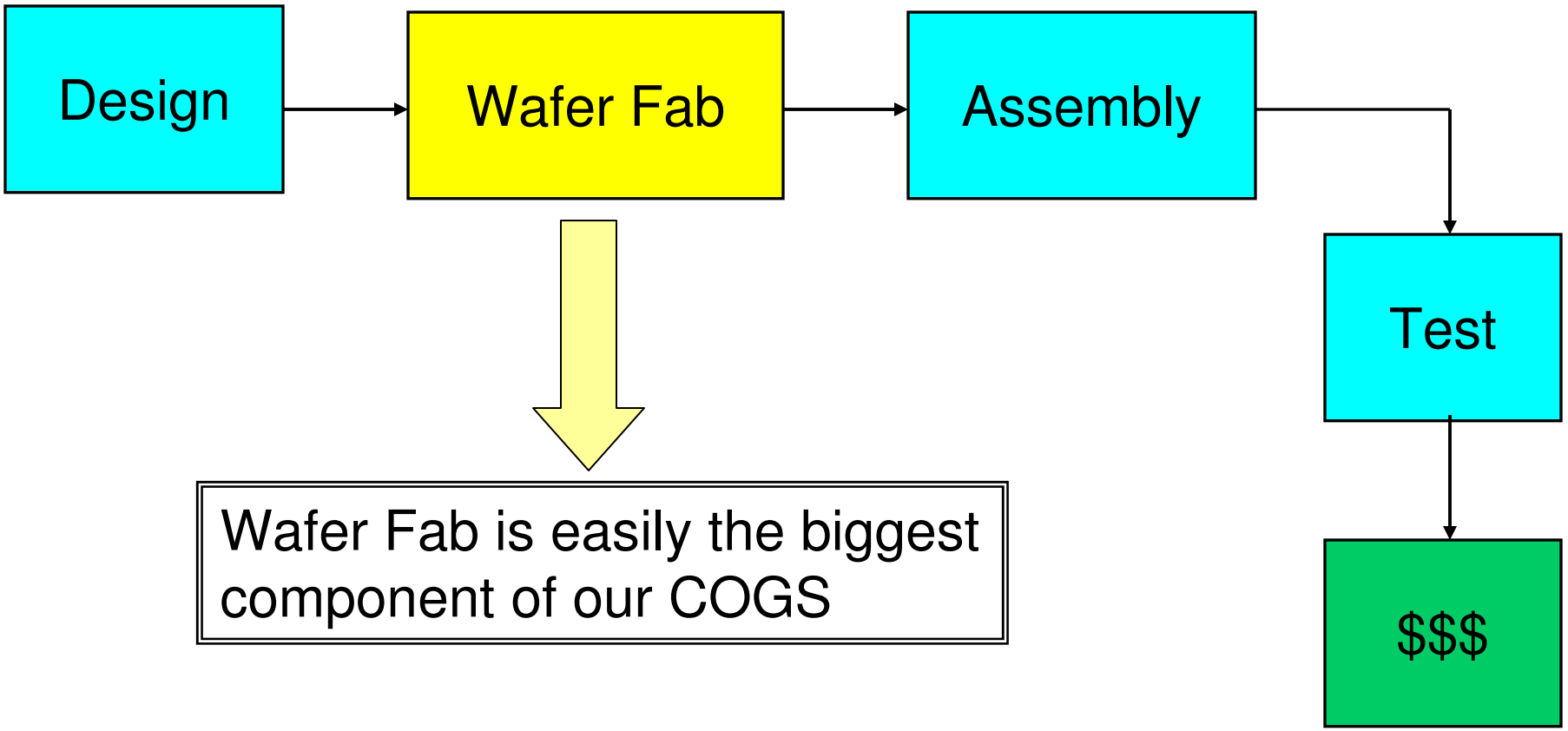
# CMOS processing

With help from David Szmyd, Silicon Labs

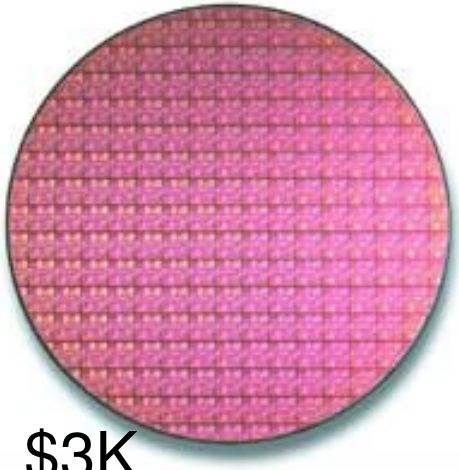
# Where Does Wafer Fab Fit into Product Flow?



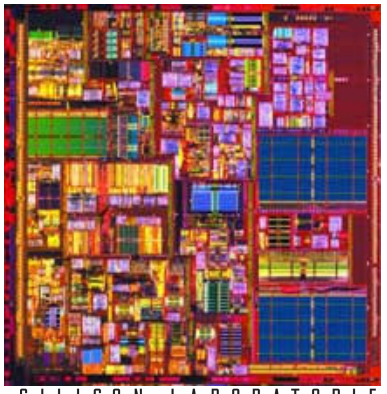
# What is a Wafer Fab?

$3B

$3M



$3K



$3

3 decades/step

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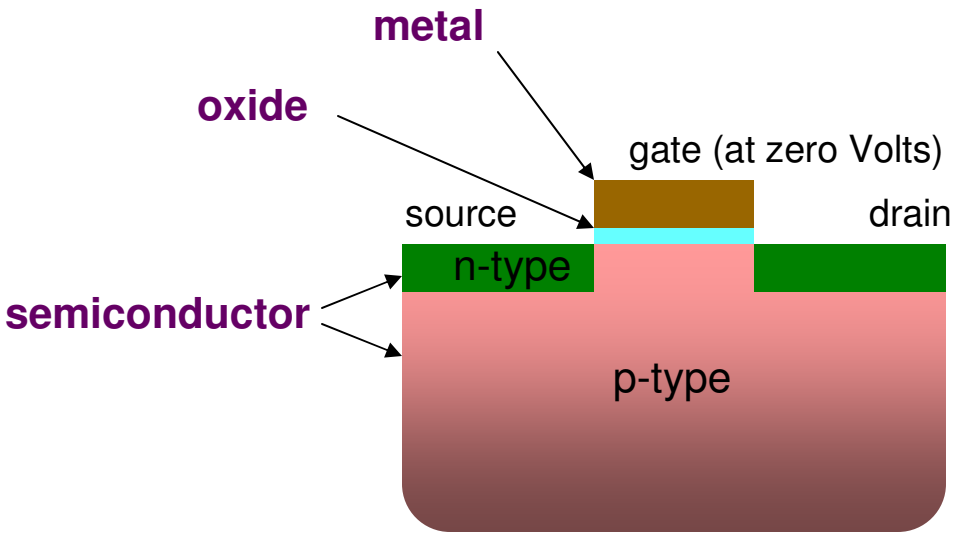
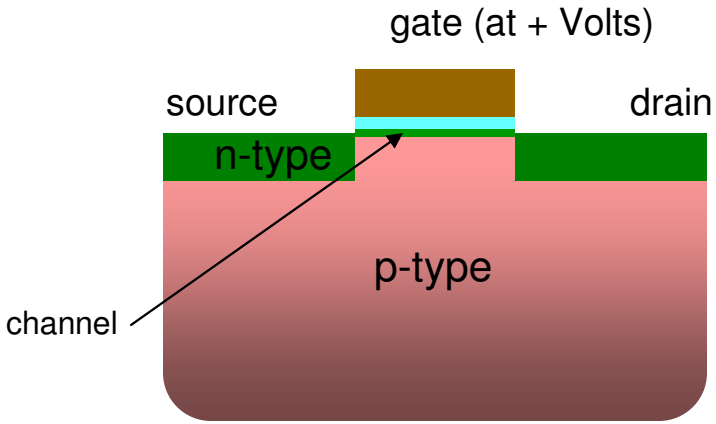
# MOS Transistor Cross Section



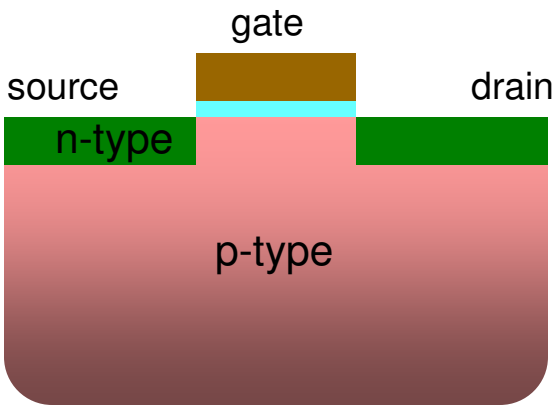

Electrons in source cannot flow to the drain because p-type region is a barrier. Transistor is OFF.



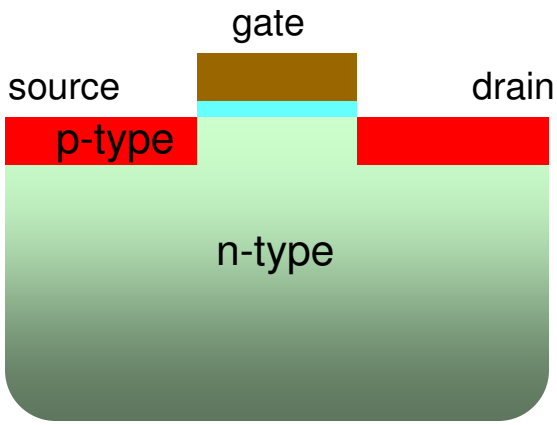

Apply positive voltage to gate. Attracts electrons to oxide, forming n-type channel. Now, electrons have a continuous path from source to drain. Transistor is ON.

# CMOS: Complementary MOS

NMOS: S, D and channel are n-type

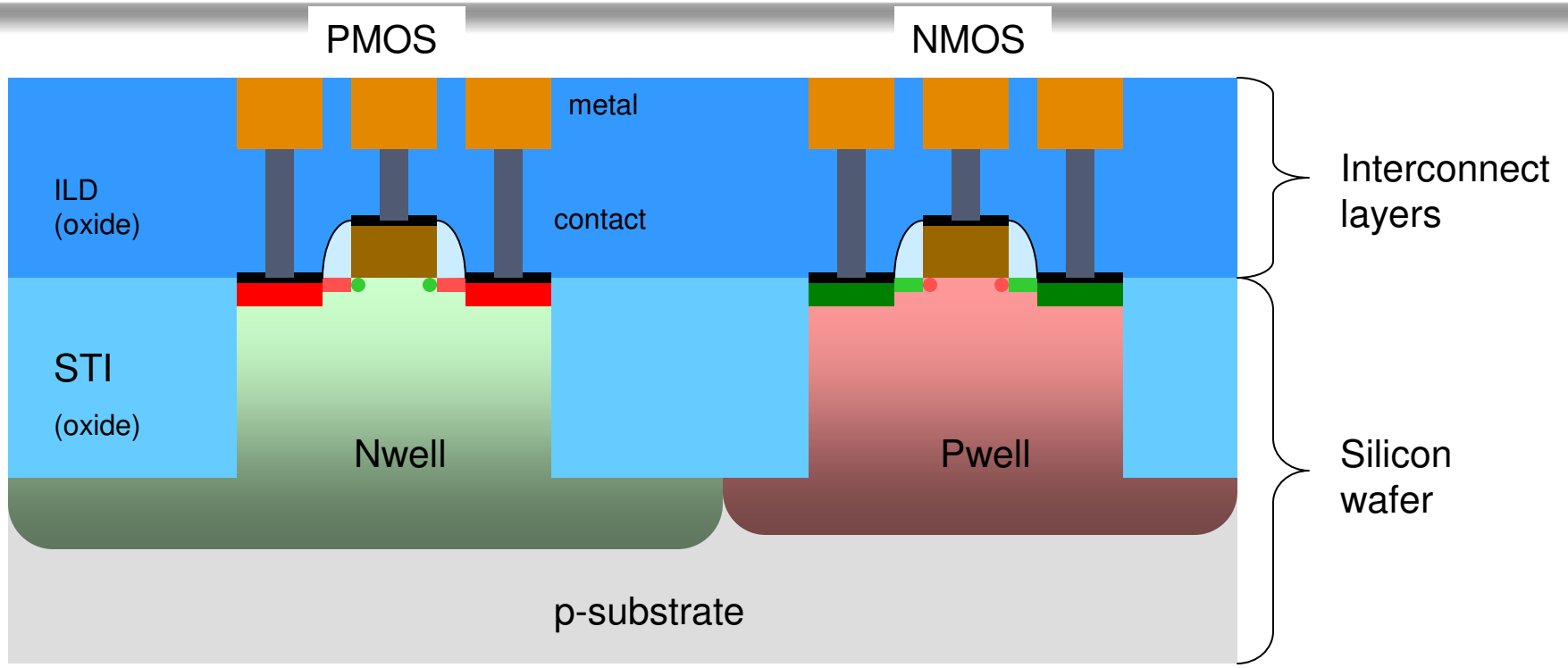



PMOS: S, D and channel are p-type




- Can combine NMOS and PMOS so that when one is on, the other is off.
  - No current flows because one device is always off. Saves power!!
  - Exception: Current flows only when devices are switching.
  - Devices are complementary → CMOS.

# CMOS Integration




- Devices are built into a common p-type substrate (wafer).
- Shallow Trench Isolation (STI) provides electrical isolation between devices.
- Metal and contacts provide access to the device terminals S, D, G.
- Multiple levels of metal lines are routed to interconnect the devices → form a circuit on a chip.
- Capacitors, resistors and inductors can also be integrated.

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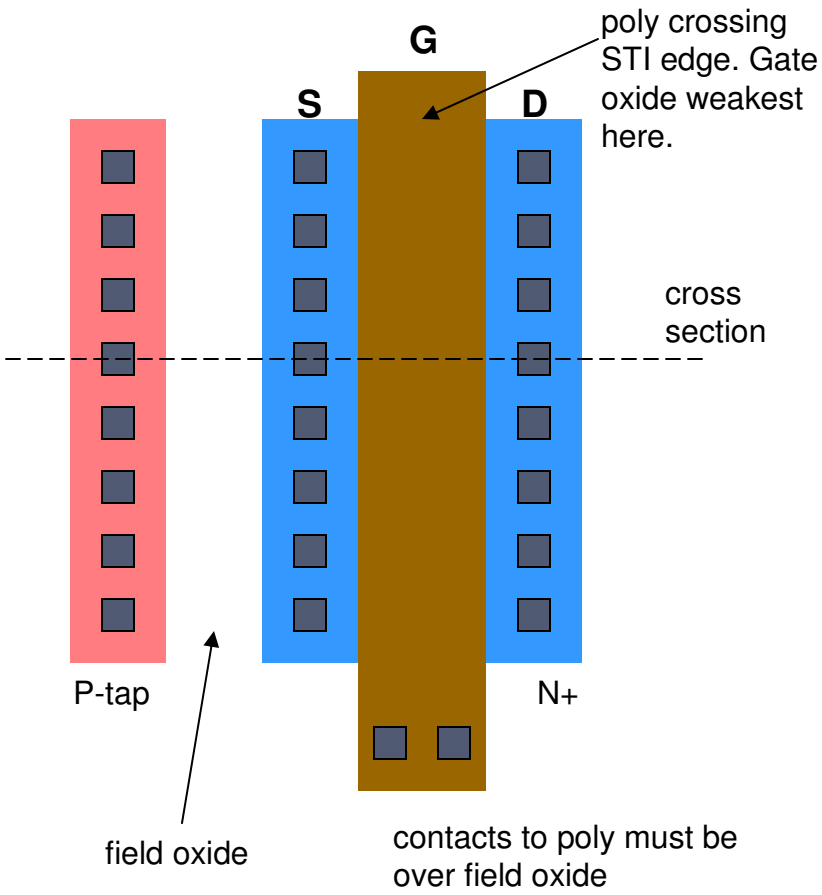
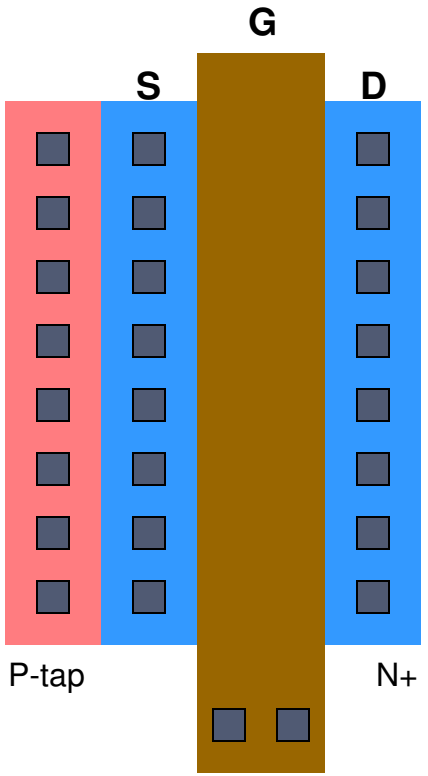
# Transistor Layout

NMOS with separate well tap

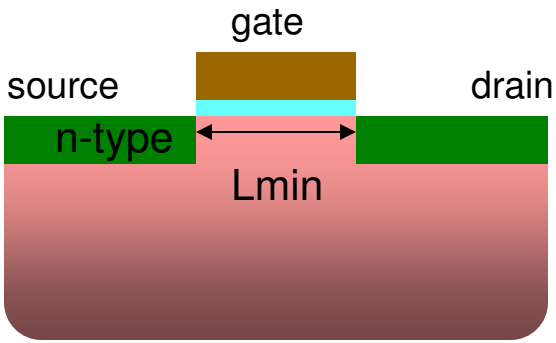



NMOS with well tap shorted to source by the silicide



# Technology Nodes

Technology defined by minimum allowed gate length.




Shorter gates → faster transistors (100 GHz) and denser circuits. Each node increases density by ~2x.

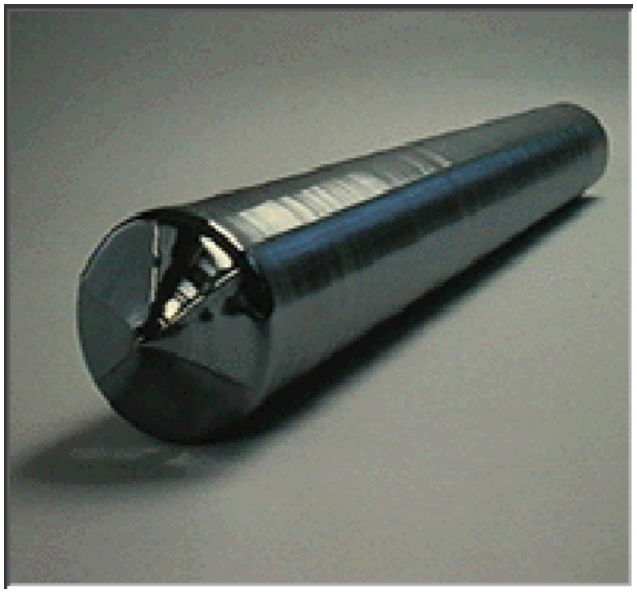
0.5µm → 0.35µm → 0.25µm → 0.18µm → 0.13µm

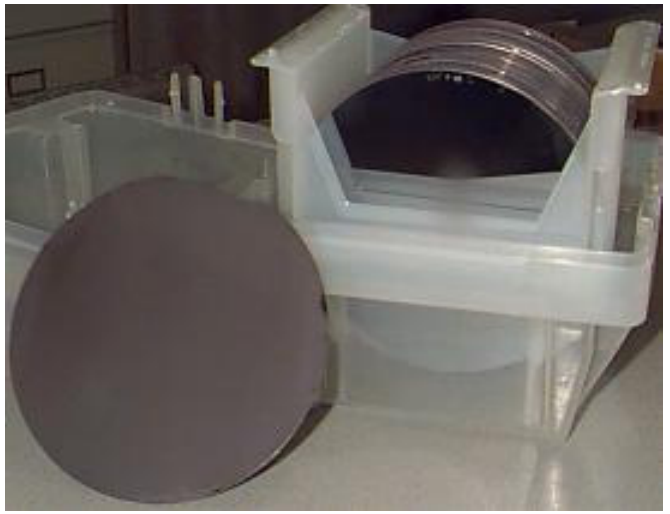
- At finer nodes, all features shrink: contact size, metal width, oxide thickness, etc.
  - In 0.13um, gate oxide thickness is only 20A (about a dozen $SiO_2$ molecules).

| Part | Function | Tech | Contact | M1 L/S | # metals | # masks | Size |
|---|---|---|---|---|---|---|---|
| chip1 | example1 | 0.5µm | 0.5µm | 0.6/0.6µm | 3 | 16 | 4.62 $mm^2$ |
| chip2 | Example2 | 0.35µm | 0.4µm | 0.5/0.45µm | 4 | 21 | 6.07 $mm^2$ |
| chip3 | Example3 | 0.35µm | 0.4µm | 0.5/0.45µm | 4 | 30 | 8.95 $mm^2$ |
| chip4 | Example4 | 0.25µm | 0.3µm | 0.32/0.32µm | 4 | 23 | 5.5 $mm^2$ |
| chip5 | Example5 | 0.18µm | 0.22µm | 0.23/0.23µm | 5 | 23 | 6.51 $mm^2$ |
| chip6 | Example6 | 0.13µm | 0.16µm | 0.16/0.18µm | 8 | 37 | 2.93 $mm^2$ |

# Wafer Fabrication

- Armed with photomasks and starting substrates, the foundry can now fabricate the wafers.
  - Starting substrates are cut and polished from huge single crystals of silicon. Not done by the foundries.





# Basic Process Steps

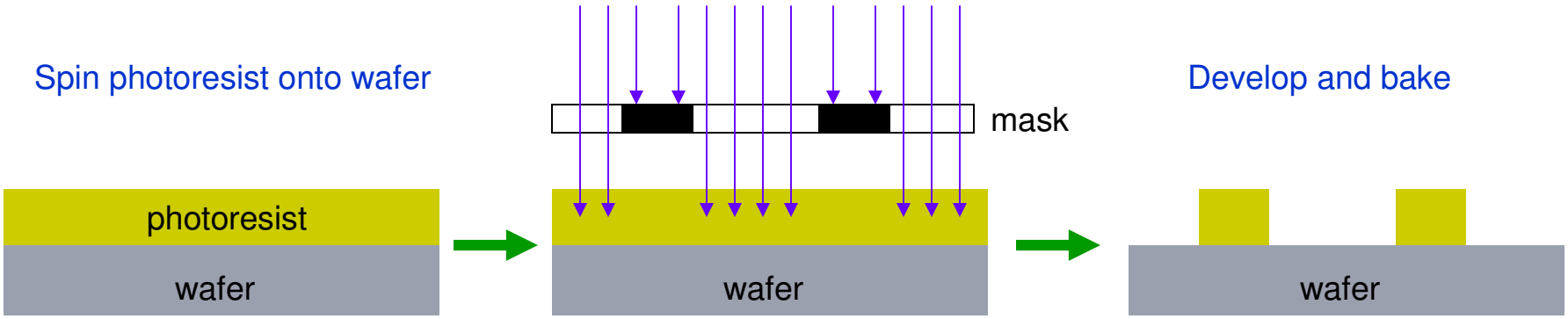
- Photolithography – transfer mask pattern to wafer
- Implant – shoot impurities into the silicon
- Diffusion – anneal implant damage, grow oxide
- Deposition – deposit layers (oxides, metals, etc.)
- Etch – remove unwanted material
- CMP – chemo-mechanical polishing. Removes unwanted material by polishing, leaving the wafer flat.

# Photolithography

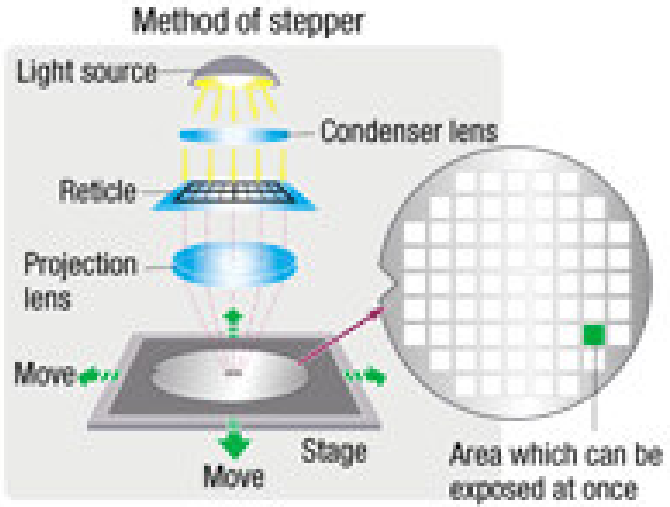
Spin photoresist onto wafer

Expose with UV light

Develop and bake




Photoresist Application
(Ontrak)




Process (etch or implant)

Strip resist

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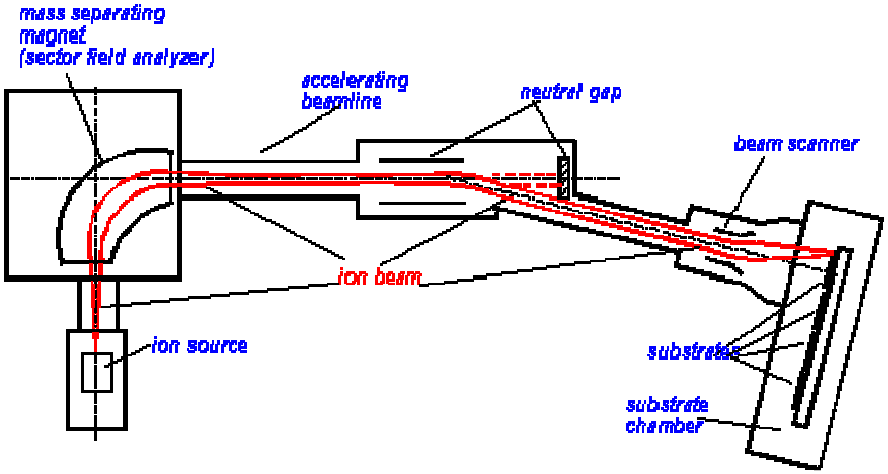
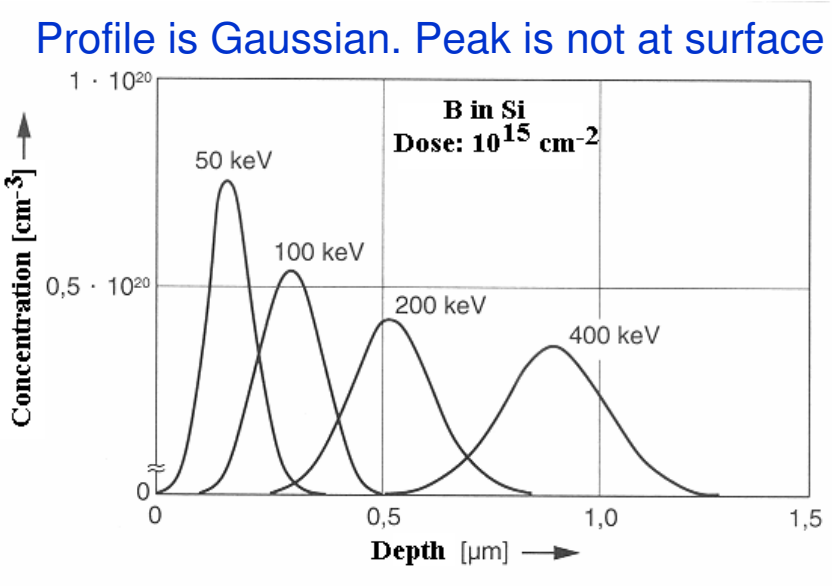
# Ion Implantation

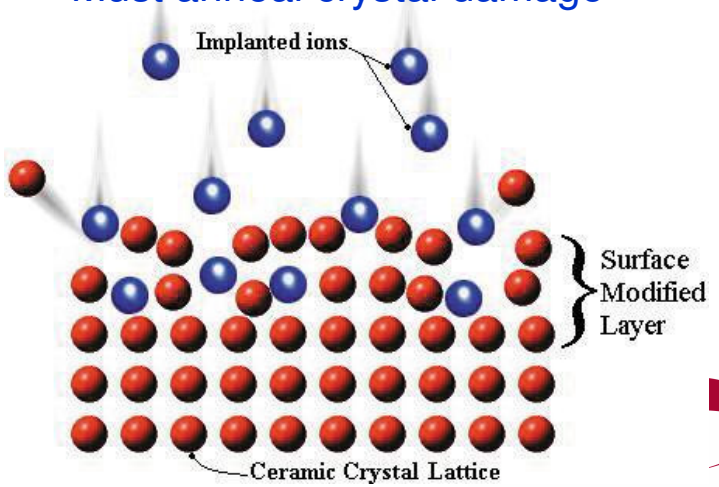
Ionize and accelerate impurity atoms into the silicon. 100eV – 1 MeV.




Profile is Gaussian. Peak is not at surface




Must anneal crystal damage

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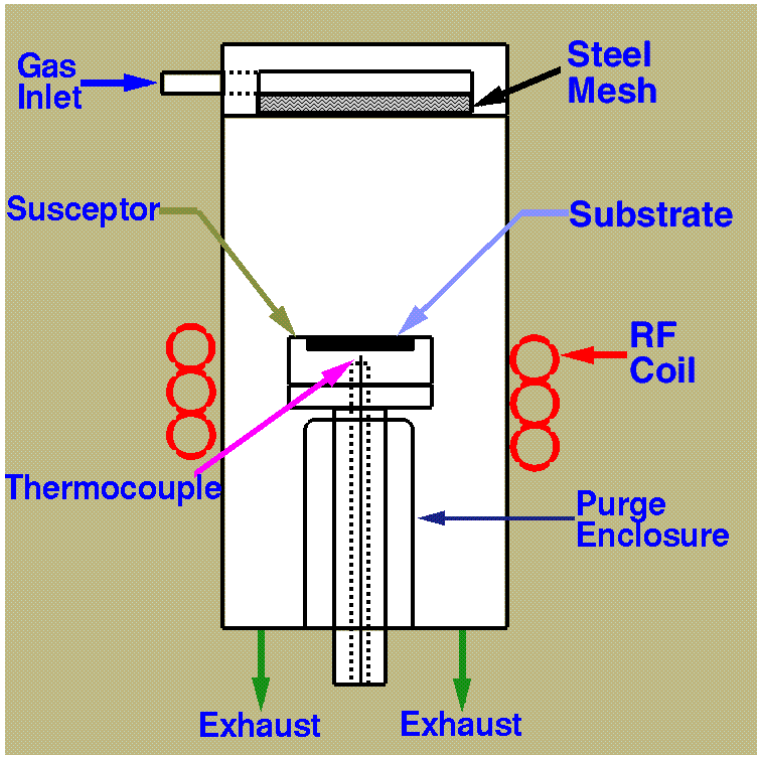
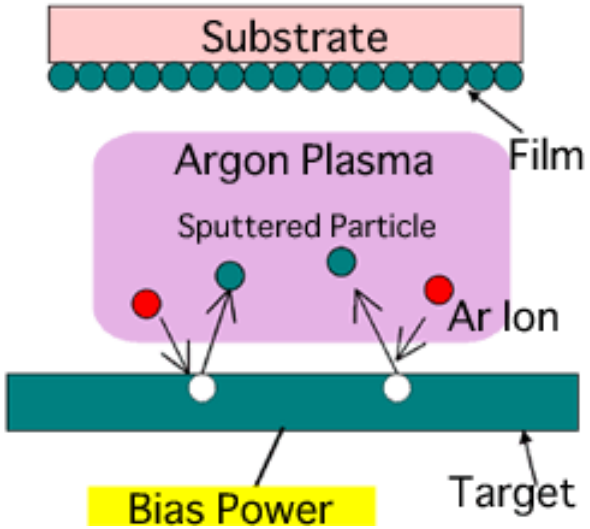
# Deposition

## Chemical Vapor Deposition




- React source gases inside chamber.
- RF plasma (usually)
- Reduced pressure
- Used for oxides and polysilicon, epitaxy.

## Sputter material from a target onto the wafer




- RF plasma + magnetron.
- Argon ions physically dislodge target atoms.
- Good for depositing metals.
- Can add $O_2$ for reactive sputtering.

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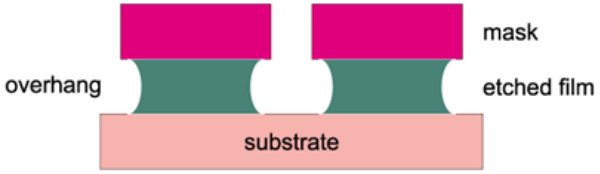
# Etch

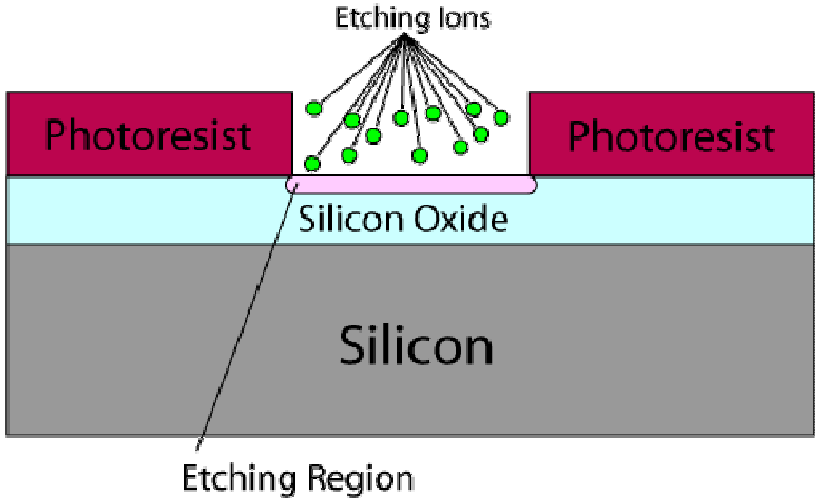
## Wet Etch

- Dip wafers boat in HF acid to remove oxide
- Isotropic

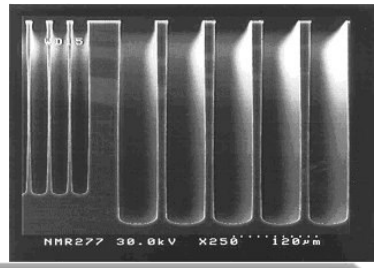



ISOTROPIC ETCHING

## RIE – Reactive Ion Etch




- Use reactive ions like $Cl^-$ or $F^-$ to etch material.
- Single wafer tool.
- Want high selectivity.
- Usually want high anisotropy.







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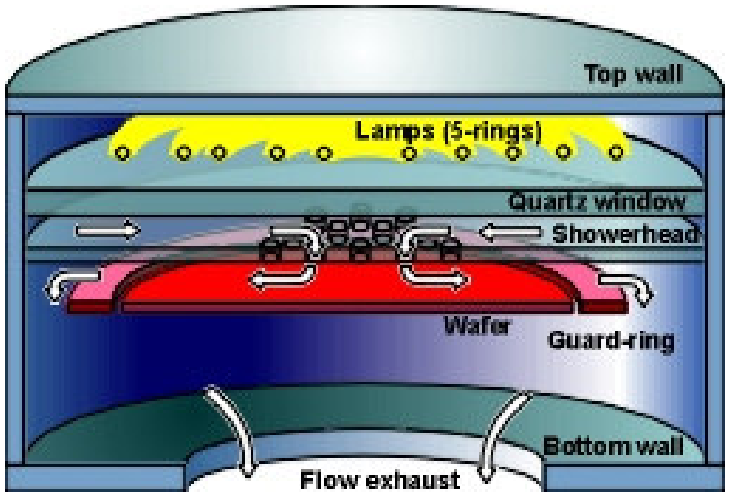
# Diffusion

## Furnace


- Used for long anneal or alloy
- Grow gate oxide
- Batch mode

## RTP- Rapid Thermal Process




- Heat wafer extremely fast with IR lamps. Soak time of a few seconds.
- Used for impurity activation. Impurities have no time to move.
- Uniform
- Can grow films
- Single wafer tool

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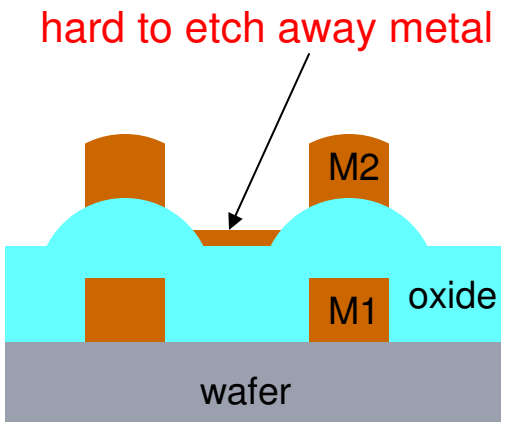
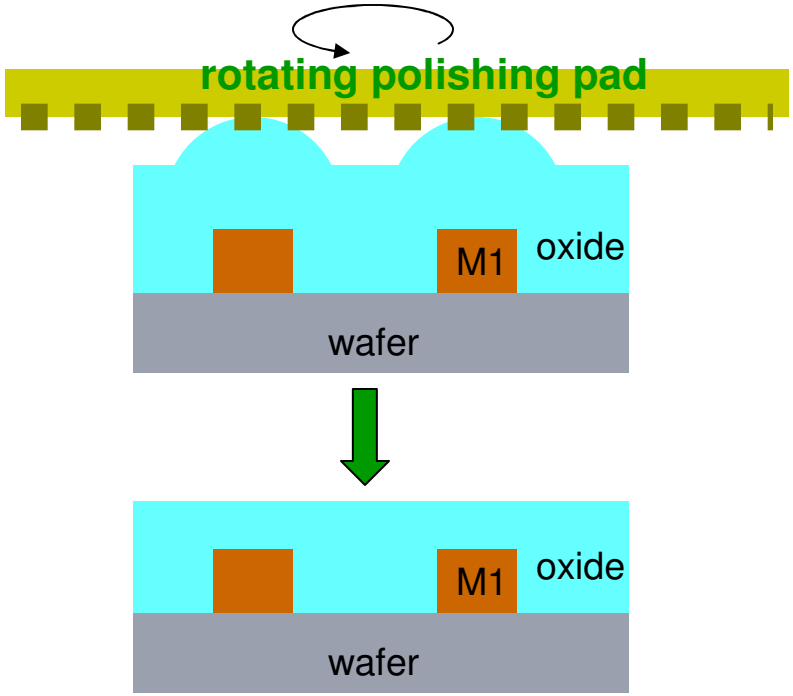
# CMP: Chemo-Mechanical Polishing

## Nonplanar wafer surface

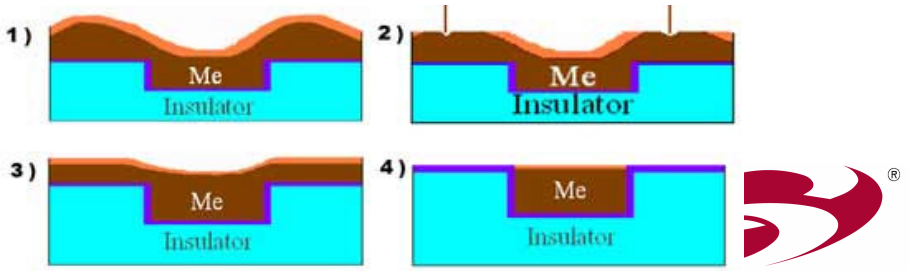



- Lowers yields.
- Limits number of interconnect layers to 2 or 3.
- Limits spacing between lines.

## Polish oxide flat first




- Can also polish metal

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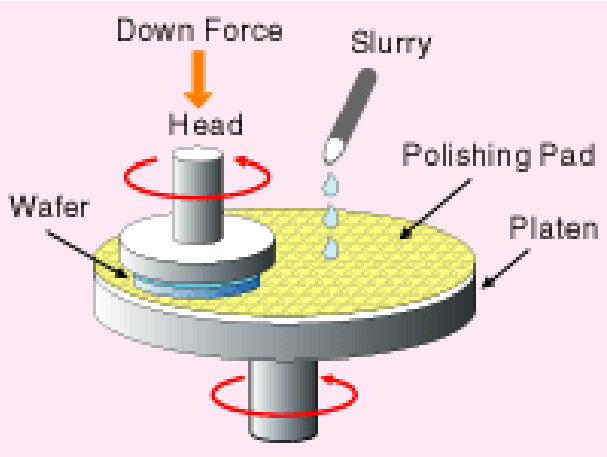
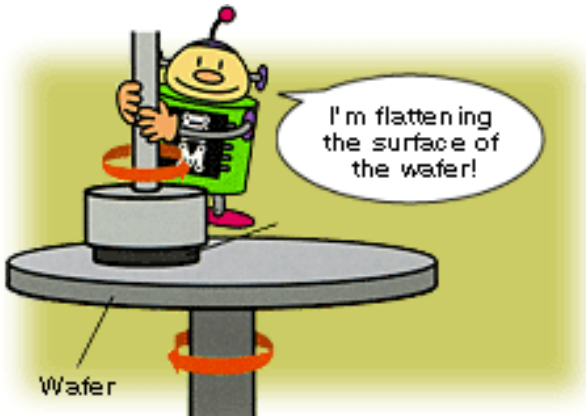
# CMP Tools

CMP Tool

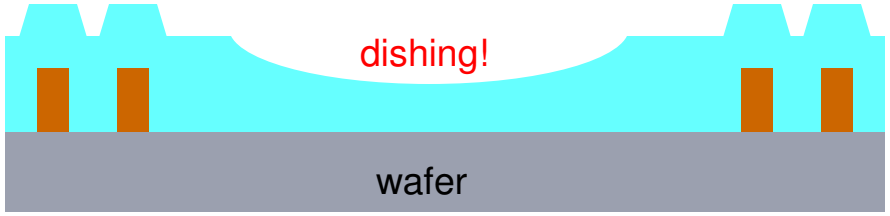


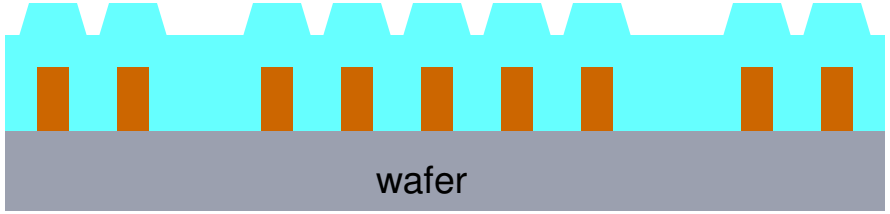

- Dirty - kept apart from other tools

# CMP Density Limitation → DFM

Large open areas get overpolished

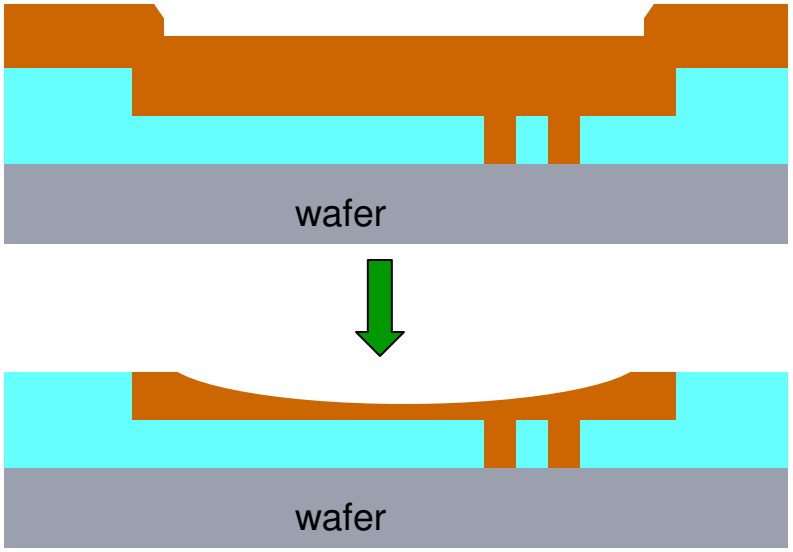



Solution. Add dummy lines to meet minimum density requirements.



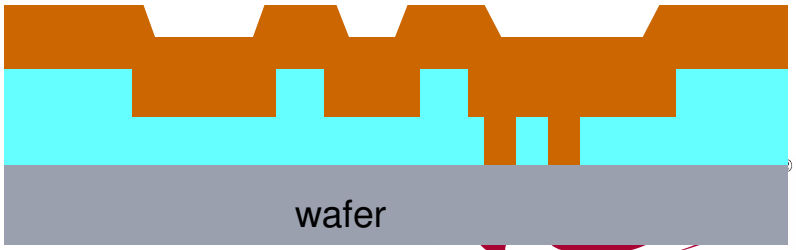

- can be done automatically
- increases parasitic capacitance

Wide metal lines get overpolished




Solution: Restrict width. Slot line.

create high points

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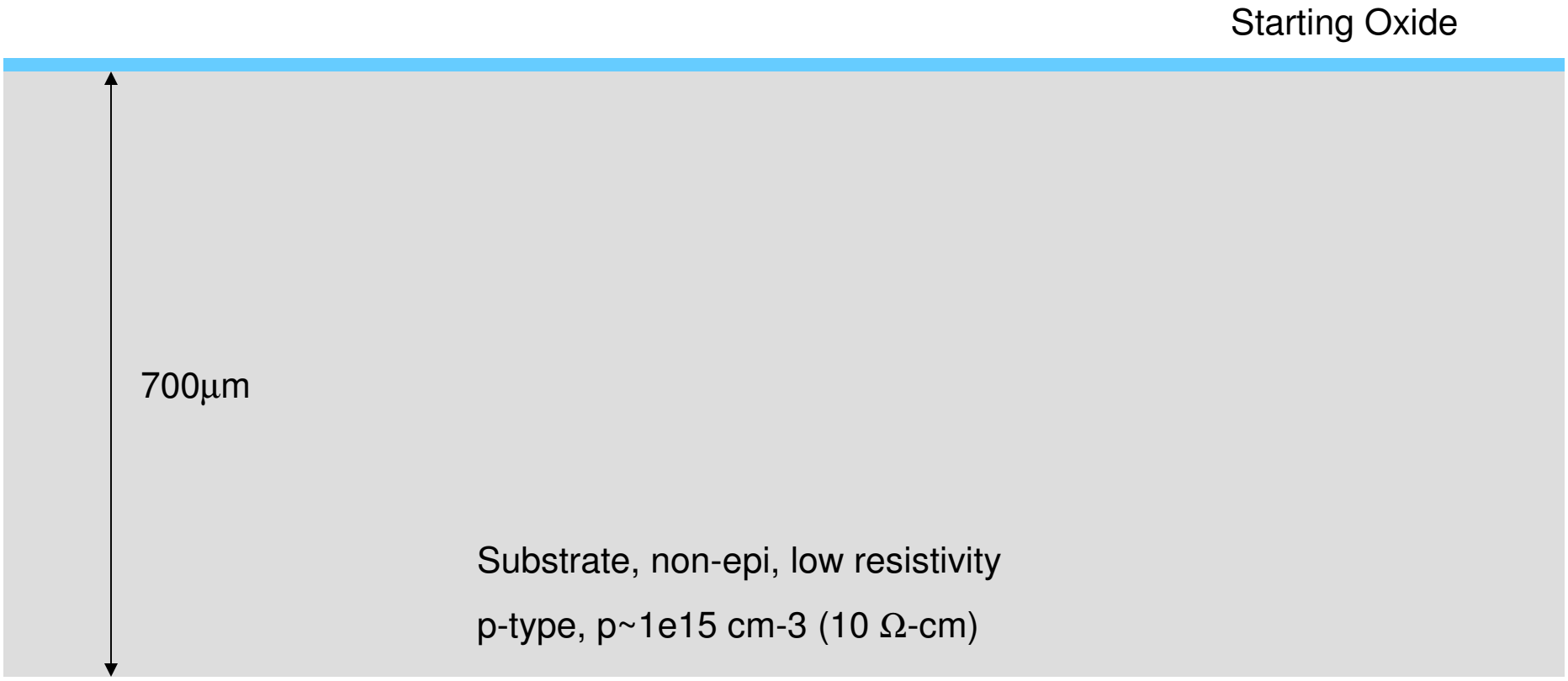
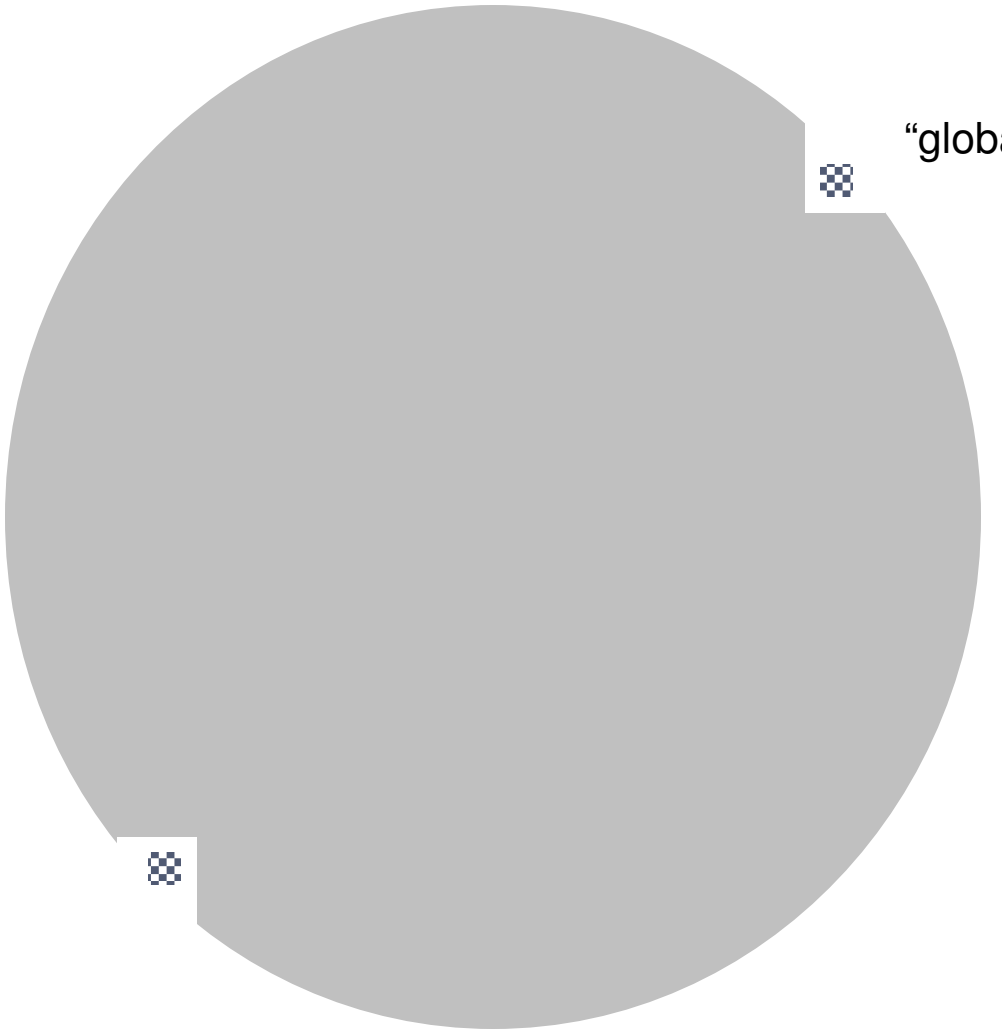
# Process Flow

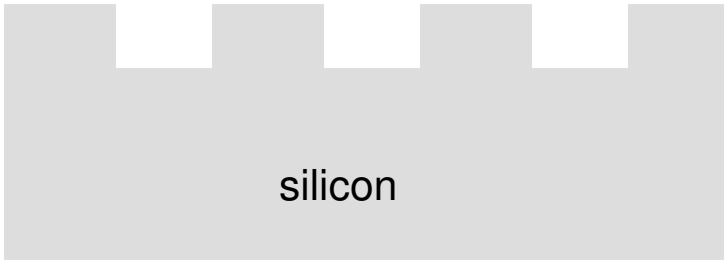
- Integrate all the previous process steps top make realize a fully processed wafer with an array of functional die.
- 0.13um process with Cu interconnect.
- Two halves
  - Frontend: from bare wafer to transistors with S/D/G electrodes.
  - Backend: interconnect layers (metals and vias) for wiring the devices.

# Starting Wafer

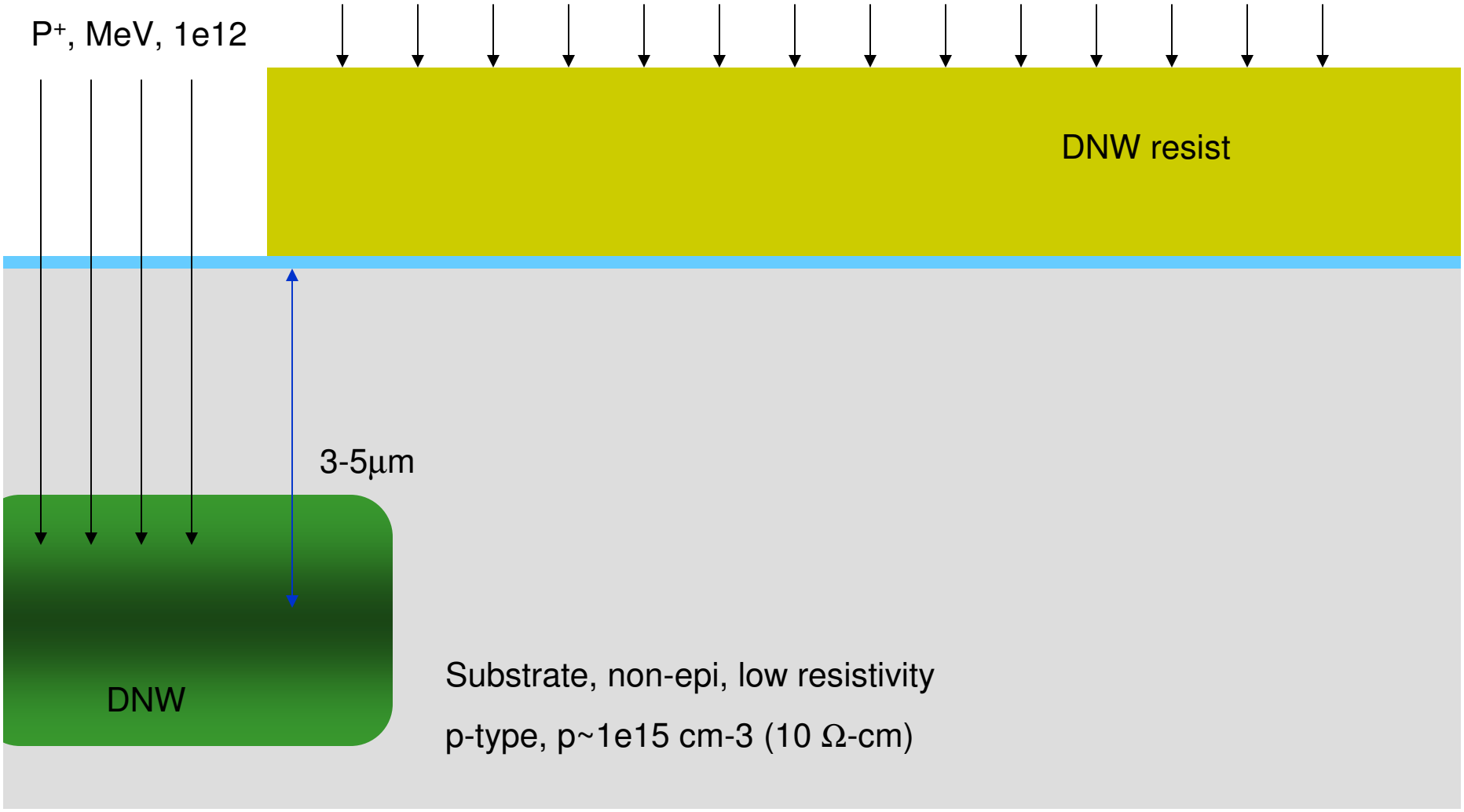


# Etch Global Alignment Marks



# DNW Mask: Deep Nwell → Isolation

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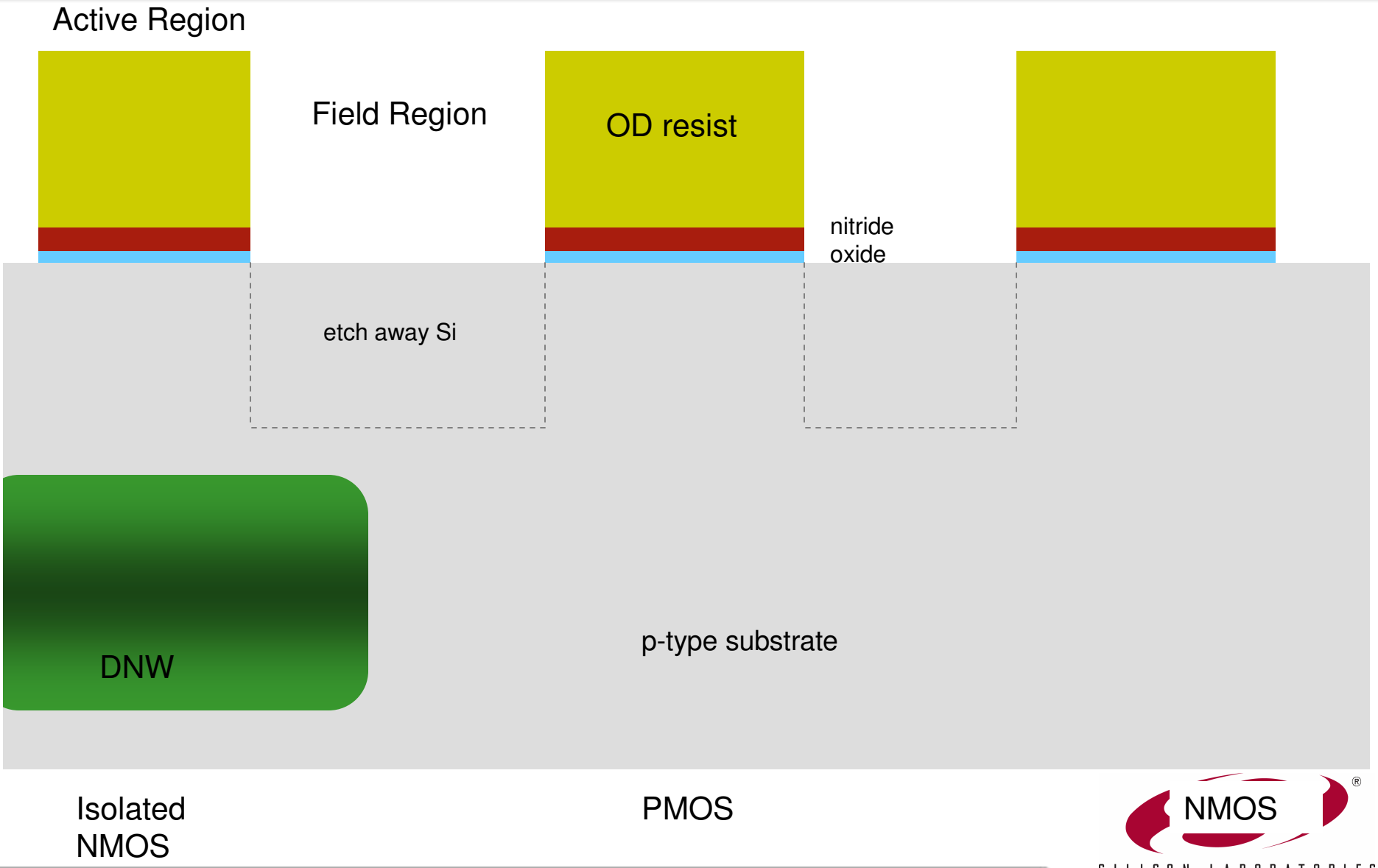
# OD Mask/Etch: Oxide Definition → Field Oxide

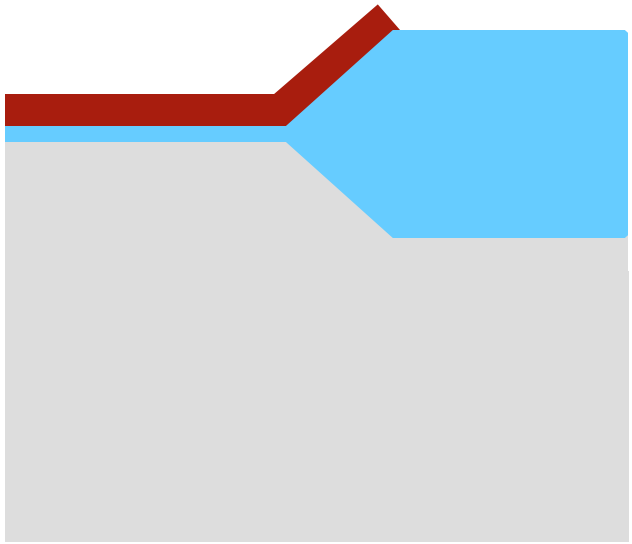


# Field Oxide: STI or LOCOS

## LOCOS

(Local Oxidation of Silicon)

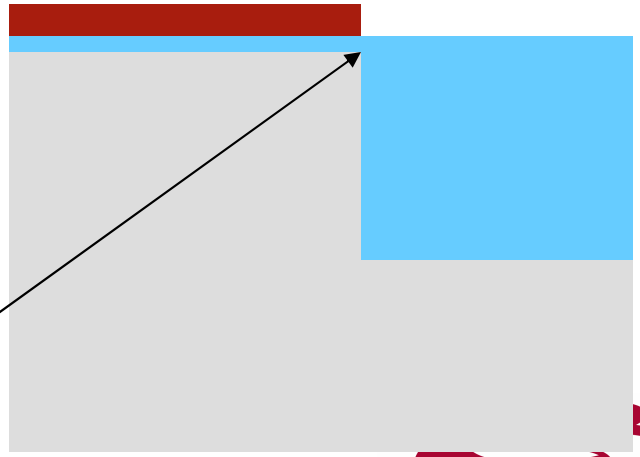
- High temperature oxidation
- Bird's beak → edge ill-defined
- Coarse pitch. No narrow field oxide
- Partially Recessed. Non-planar
- Old, 0.35um and higher



## NEW: STI

(Shallow Trench Isolation)

- Si etch, Oxide overfill, CMP back
- Flat, planar
- Low temperature
- Fine pitch
- New, 0.25um and lower

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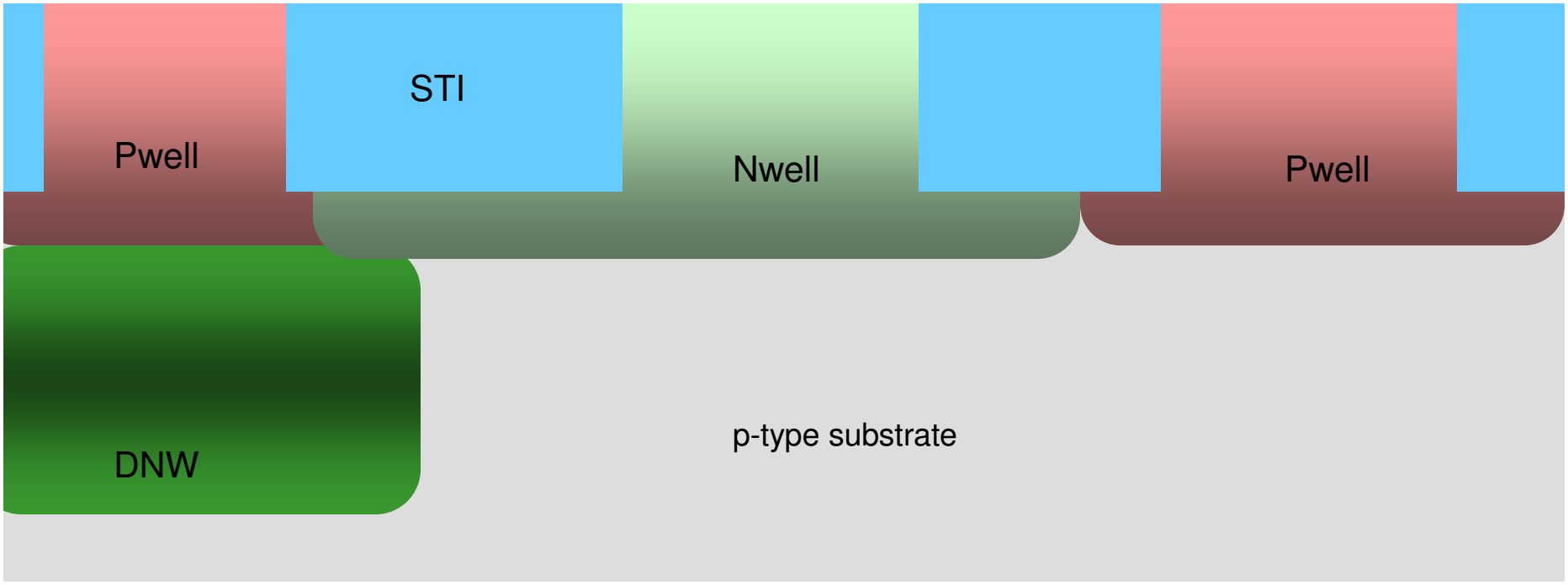
# PW and NW Masks: Nwell and Pwell Formation

- 2-3 implants/mask, B/In for Pwell, As/P for Nwell
- If process has dual Vdd, then core and I/O have separate wells
- Also, Vt adjust implants for LV and HV flavors of core transistors

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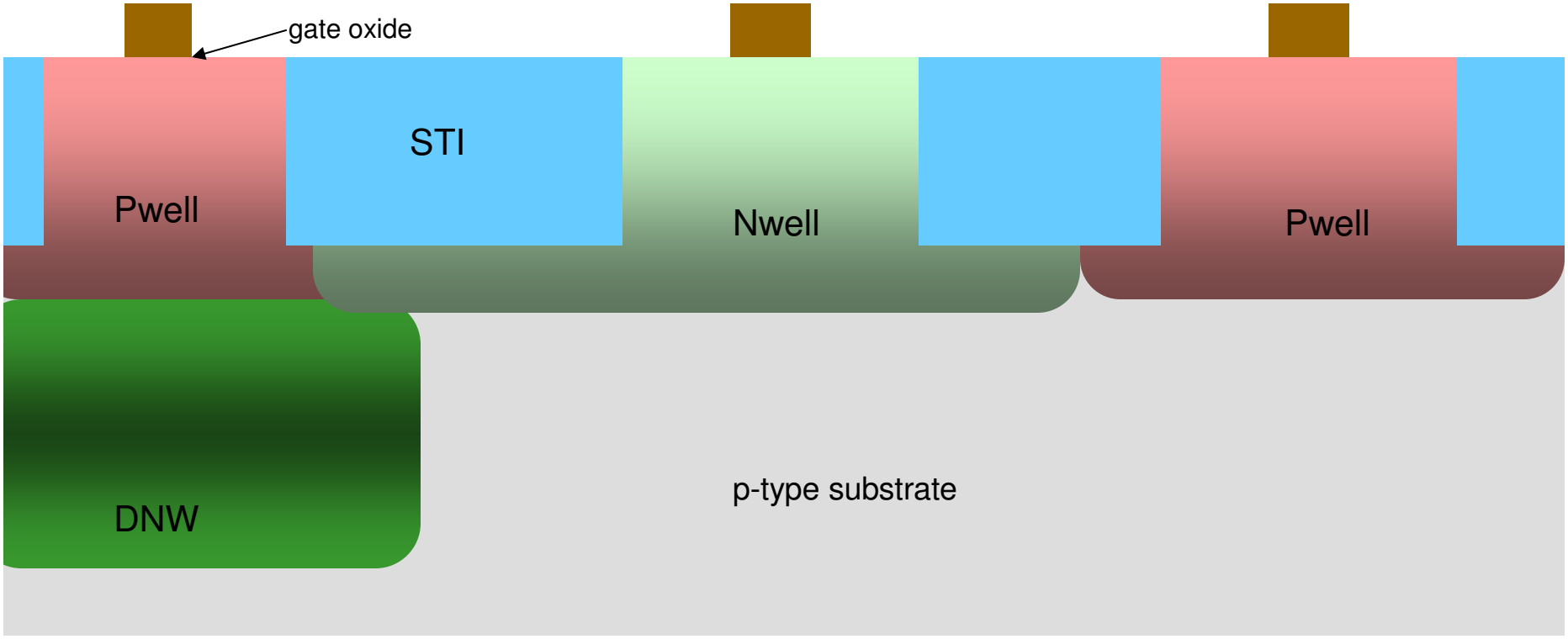
# Gate Oxide and Poly

- Grow gate oxide (could be dual oxide)
- Deposit Polysilicon (gate material)
- Etch Poly. Width is the transistor L. Control is critical (CD = Critical Dimension)



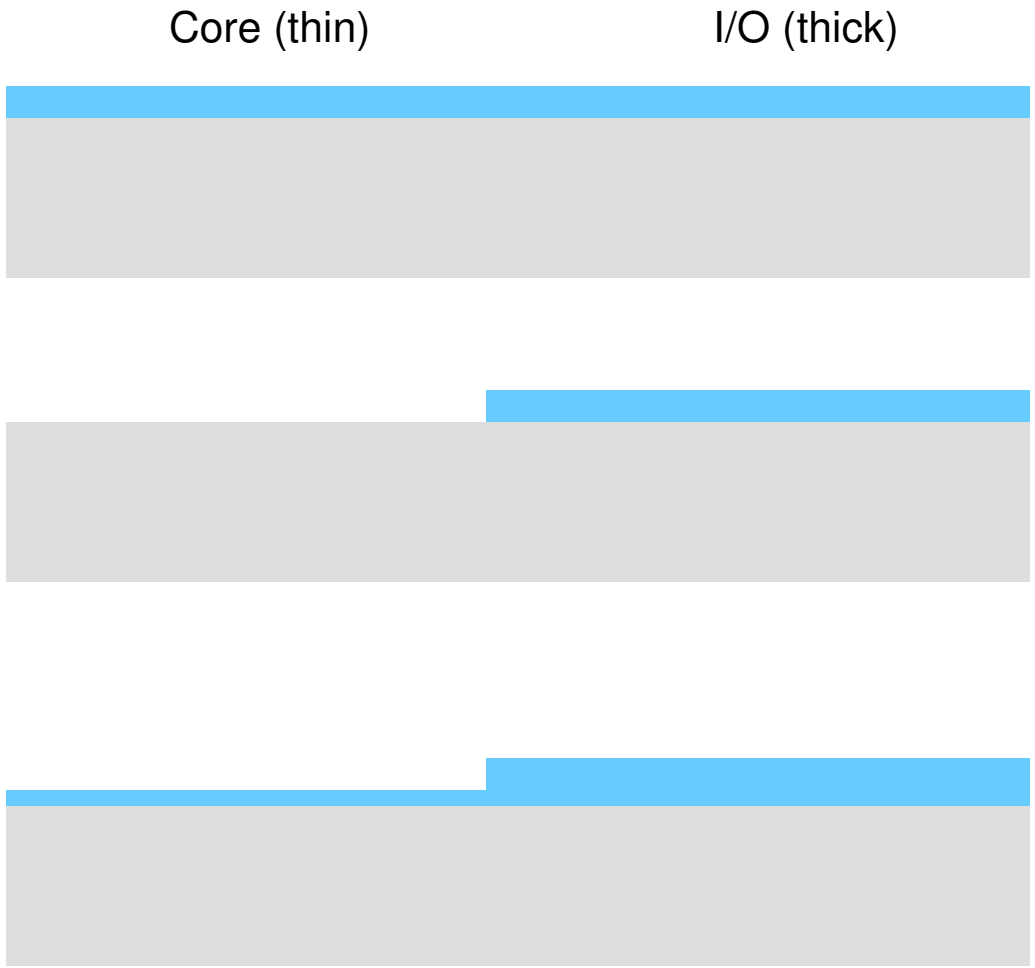
# Dual Gate Oxide: Core and I/O Transistors

- Grow partial oxide

- Remove oxide in core region (mask I/O)

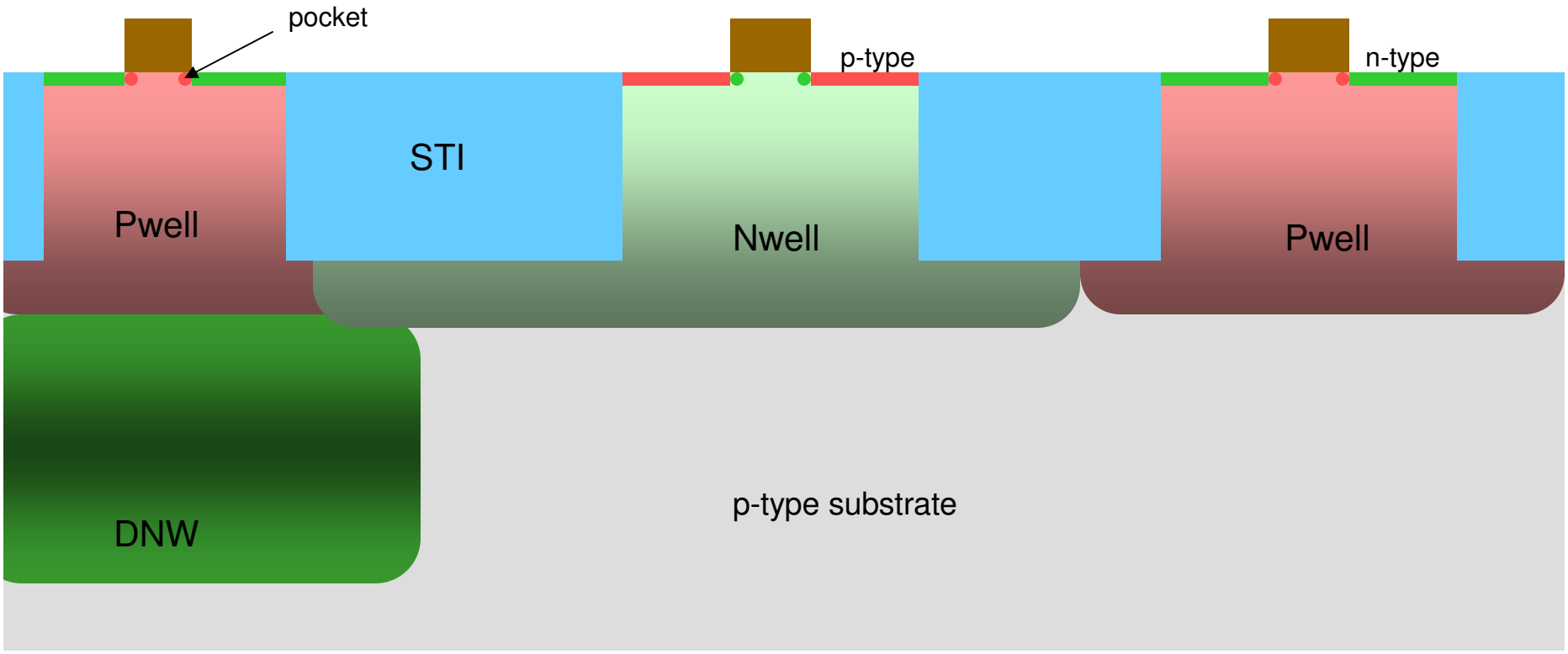
- Grow 2nd oxide

- Deposit Poly



# LDD and Pocket Implants

- Self-aligned to gate poly.
- Pocket: extra well doping to prevent Vt rolloff. Angled to get under gat poly.
- LDD: Lightly-Doped Drain. Reduces electric field and hot-carriers at drain.

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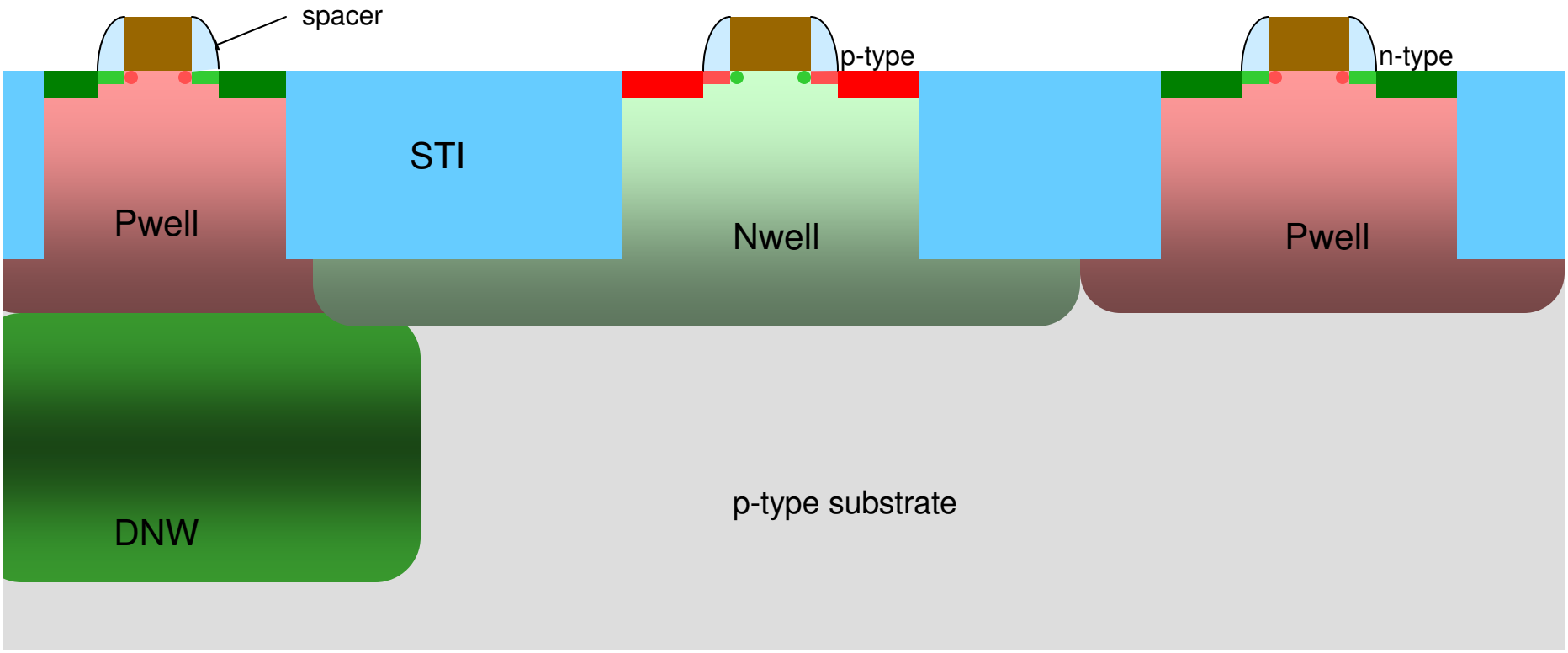
# Spacer and Extrinsic Drain

- Spacer protects LDD. About 0.1um – 0.2um wide.
- Spacer: TEOS only or nitride/oxide bilayer stack.
- Heavy extrinsic implants for low Rseries. Also dopes the poly.

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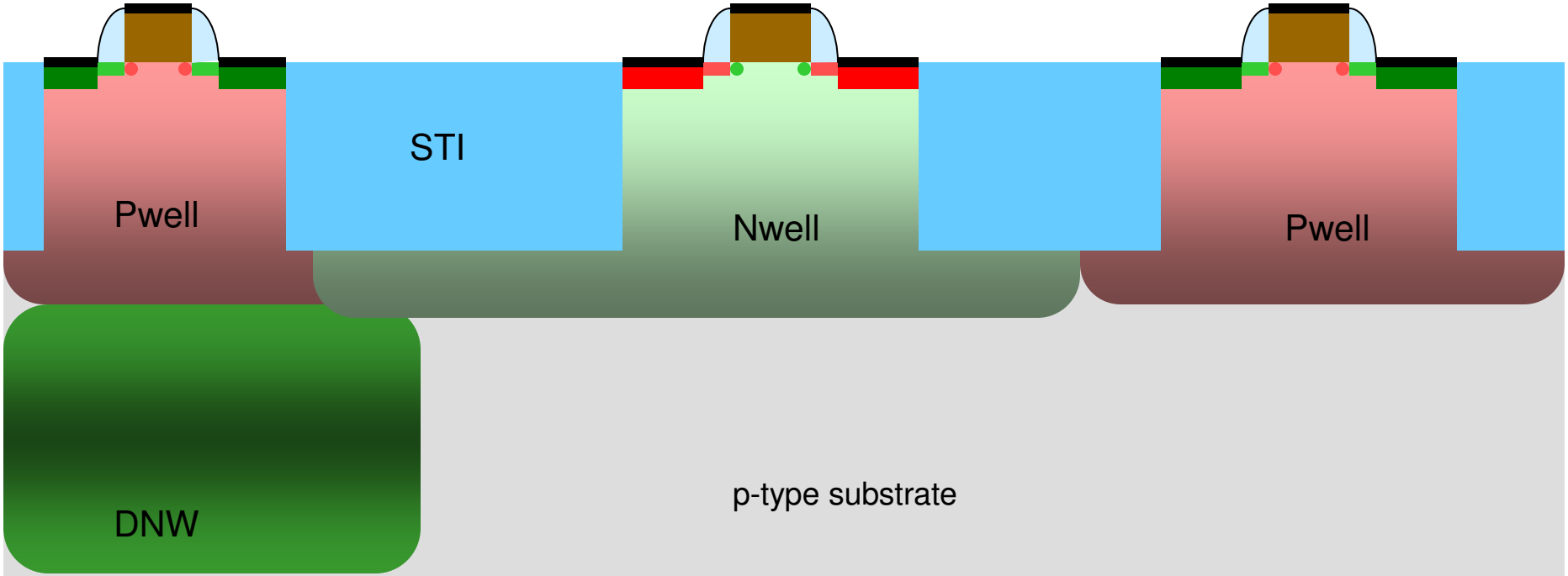
# Silicide Formation

- Self-aligned to diffusion regions and poly.
- TiSi (0.25um and above), CoSi (0.18um to 90nm), NiSi (65nm)
- Deposit → React → Strip → Convert to low resistance phase



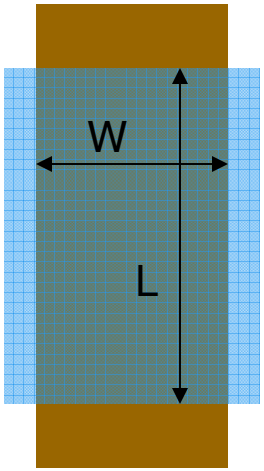
# Prevent Silicide with RPO Layer

- Before sputtering silicide metal, deposit oxide.
- Remove oxide where silicide is needed. Block oxide etch with RPO mask for resistors.

before strip

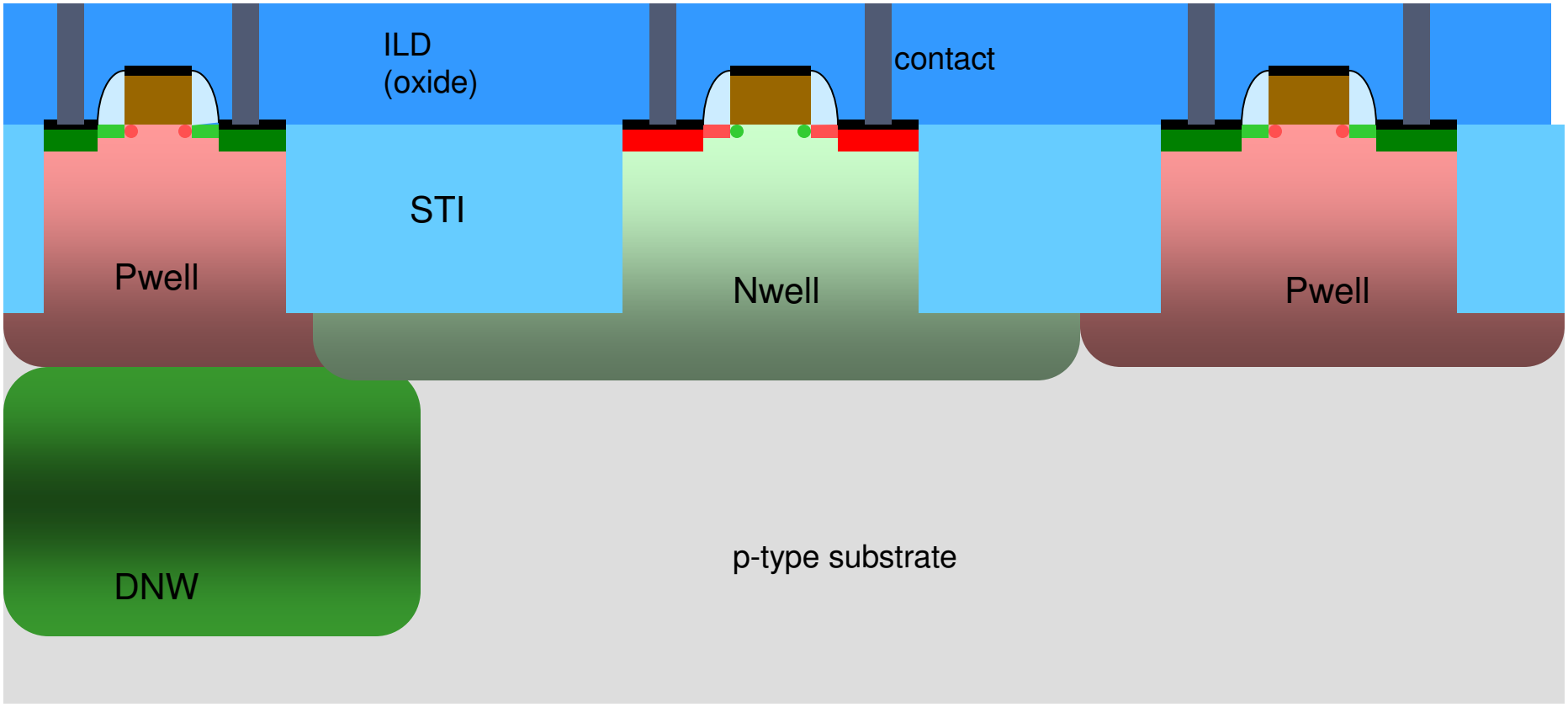
after conversion

resistor top view



# Contact Formation

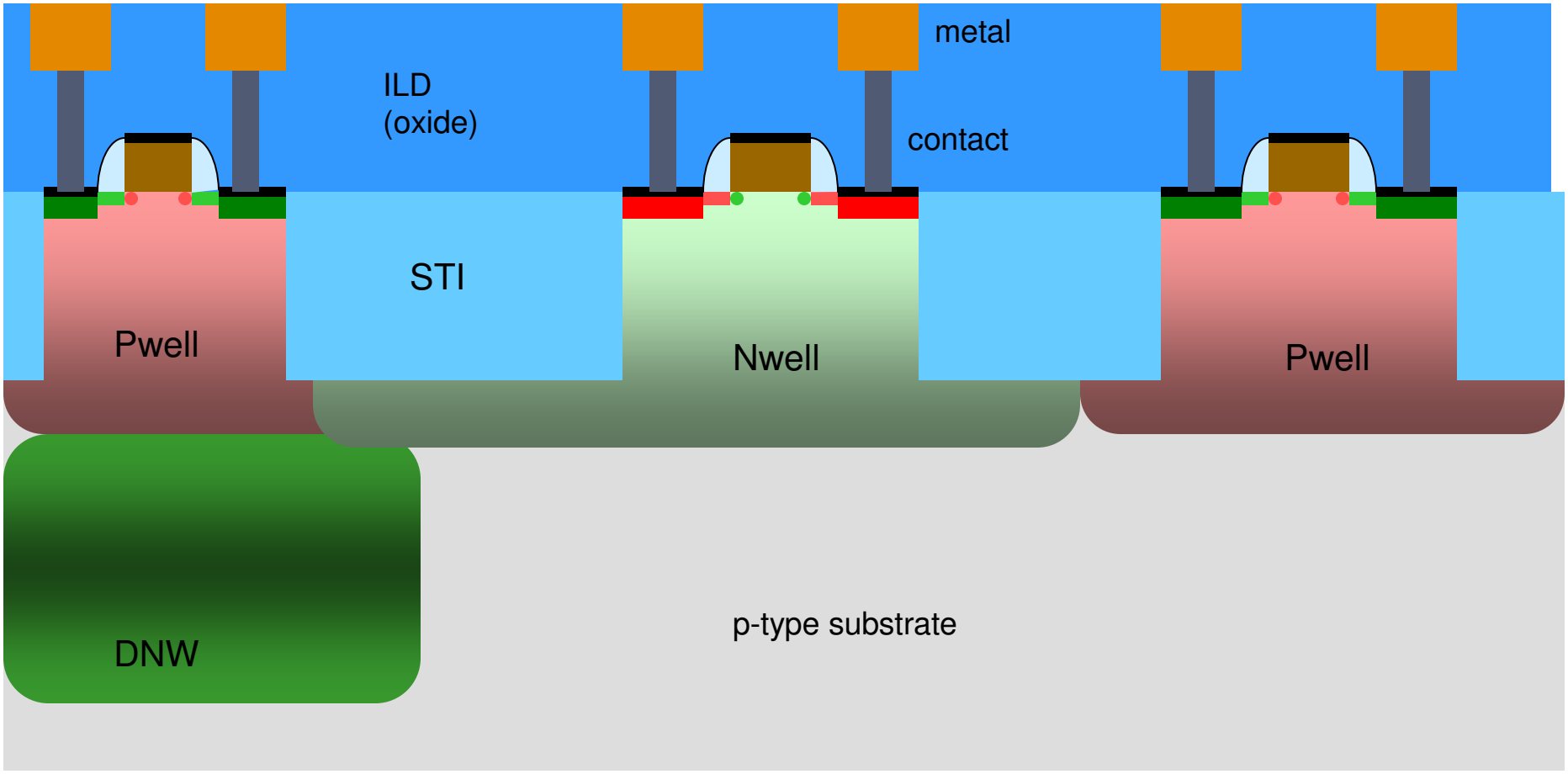
- Deposit ILD oxide and CMP flat
- Usually W-plug
- Etch hole → Deposit W → CMP flat




SILICON LABORATORIES

# Metal1

- Aluminum: Deposit metal, mask and etch.
- Copper: Deposit oxide (IMD), etch trench, deposit metal, CMP flat




Isolated NMOS

PMOS

NMOS

SILICON LABORATORIES

# Processing of Al and Cu Metal Lines

## Aluminum

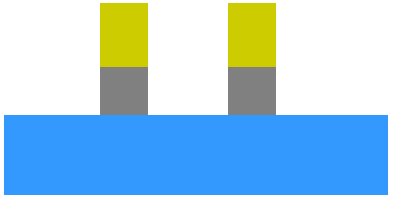
start with flat oxide

sputter Al film

pattern photoresist

etch Al

hard to etch fine lines



strip photoresist

## Copper

start with flat oxide

pattern photoresist

etch trenches in oxide, strip resist

easy to etch oxide

electroplate Cu

CMP Cu flat

SILICON LABORATORIES

# Processing of W and Cu Vias

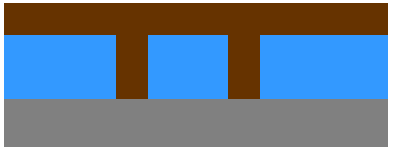
## Tungsten

start with flat oxide on top Al

pattern photoresist

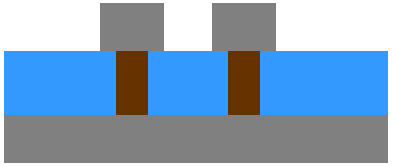
etch holes in oxide, strip resist

deposit W



CMP W flat

deposit and pattern Al lines



## Copper

start with flat oxide on top Cu

pattern photoresist

etch holes to etch stop layer, strip resist

pattern and etch metal line trenches

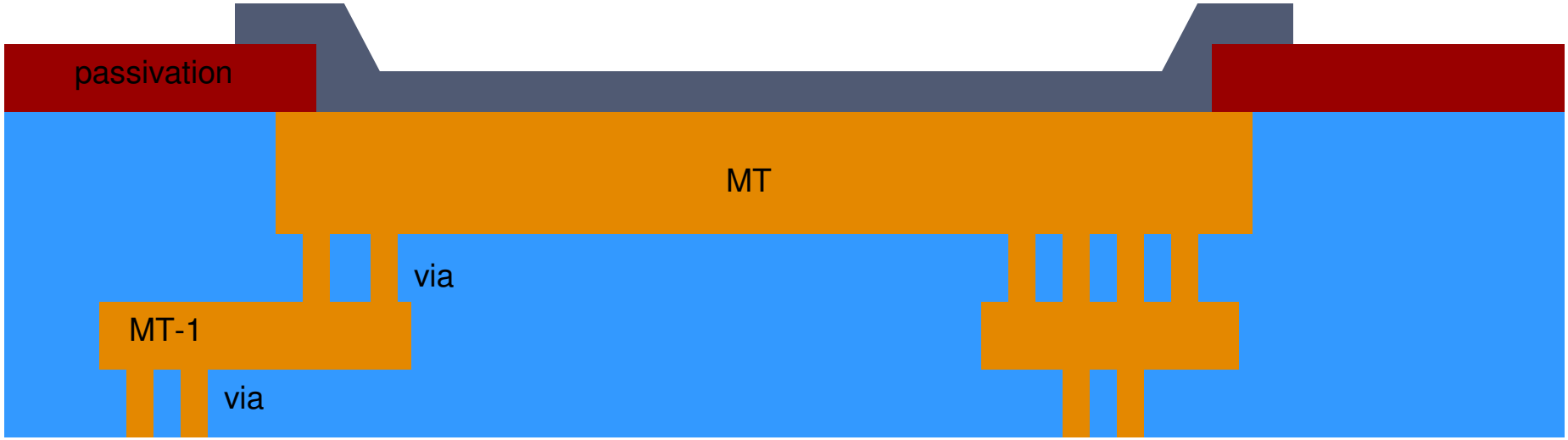
electroplate Cu

CMP Cu flat

SILICON LABORATORIES

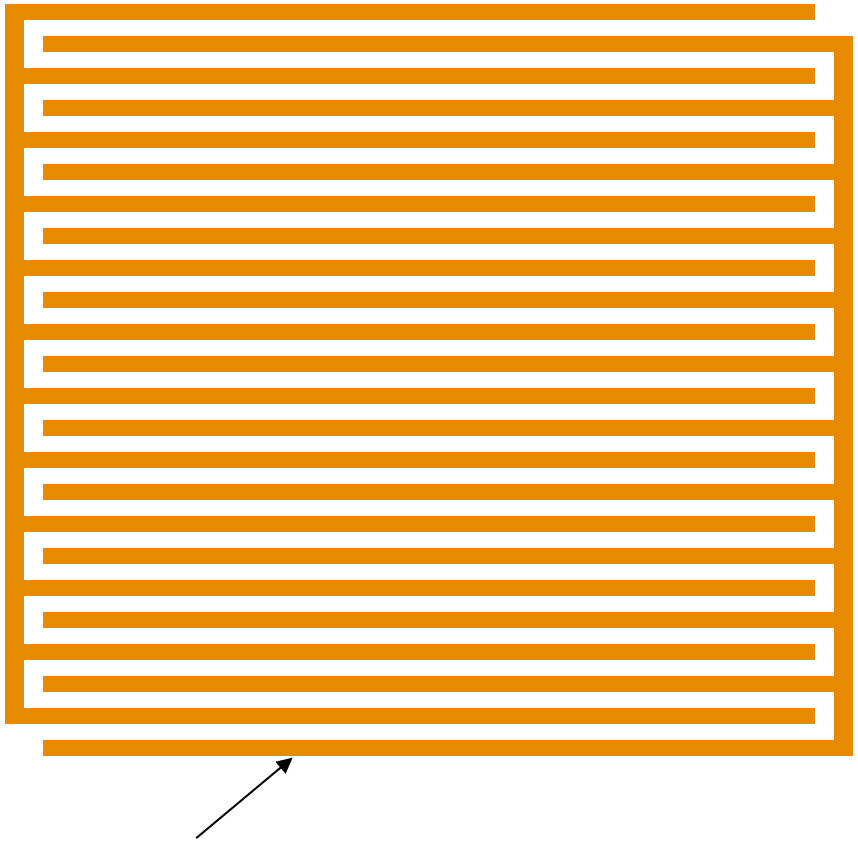
# Passivation and bondpads

- Repeat metal and via processing steps to complete interconnect.
- Deposit passivation (nitride) and etch.
- For Cu, deposit Al wirebond layer and etch.
- For P49, route Al layer to bump (redistribution of bondpads)



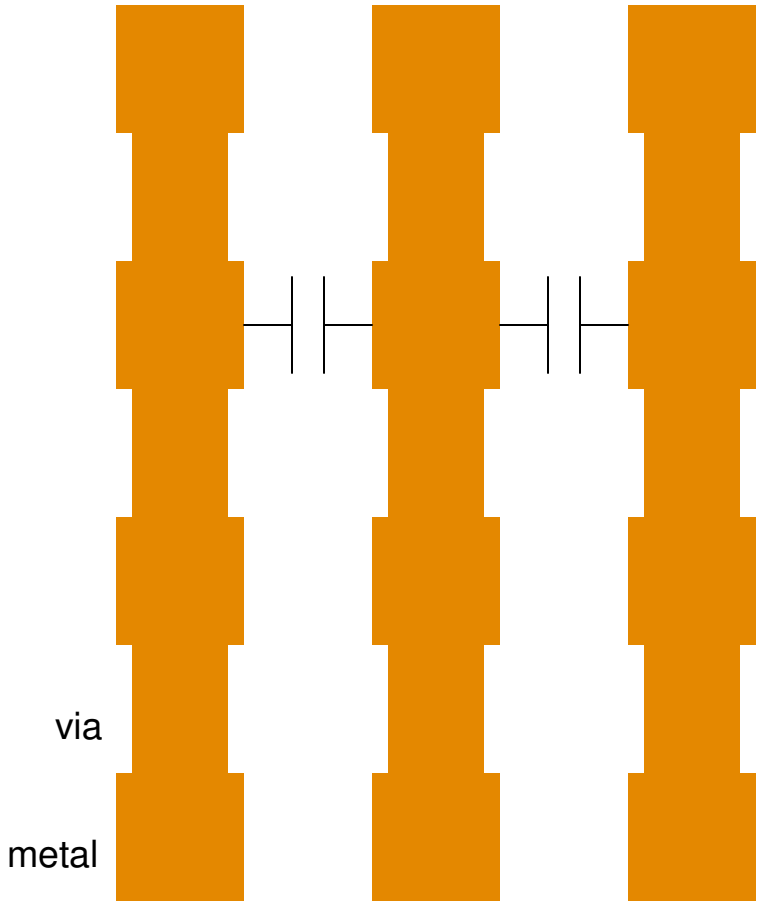
# Metal Finger Capacitors

Top View



M1-M5 stacked and tied together with vias

Cross Section (4 metal stack)

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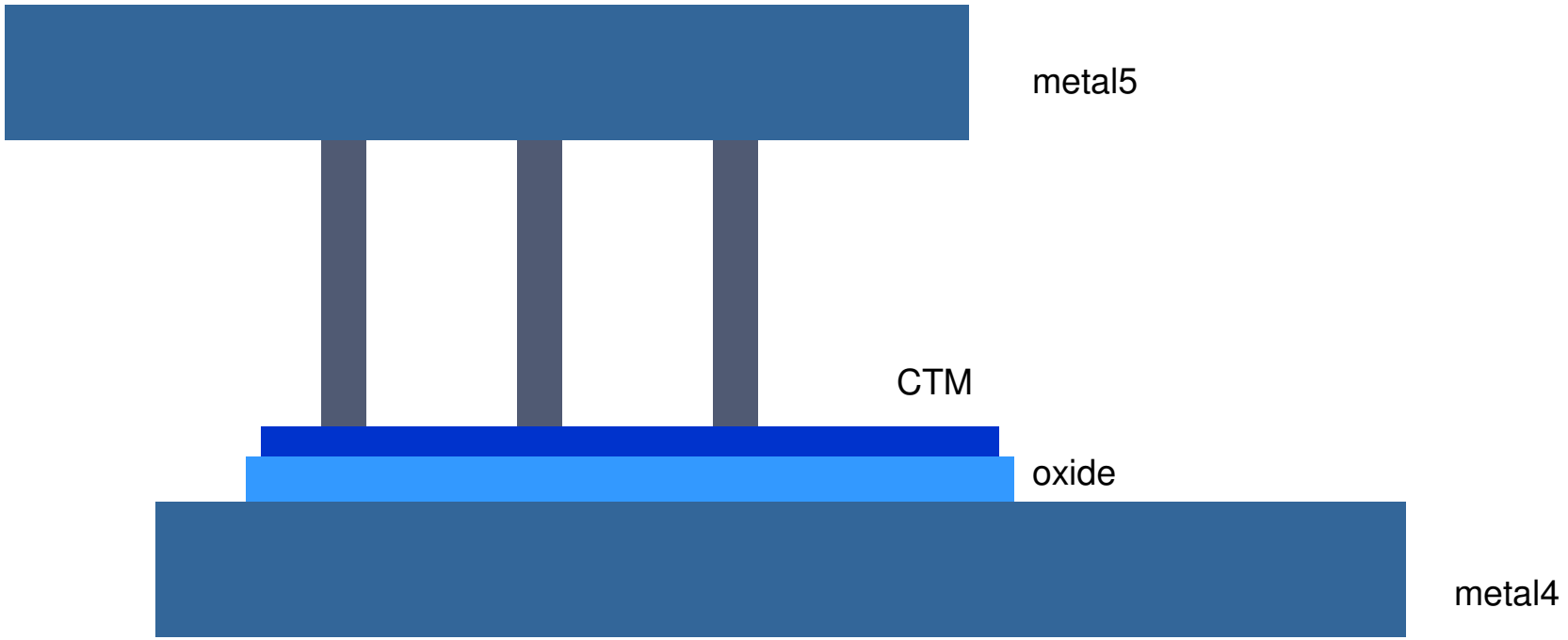
# MIM Capacitor




- Above MIMcap uses existing metal for bottom plate. This style found in 0.18um and higher. Requires one mask for CTM
- For 0.13um process, cannot use copper as a bottom plate. Instead, separate CBM layer is added. Two masks required.

SILICON LABORATORIES